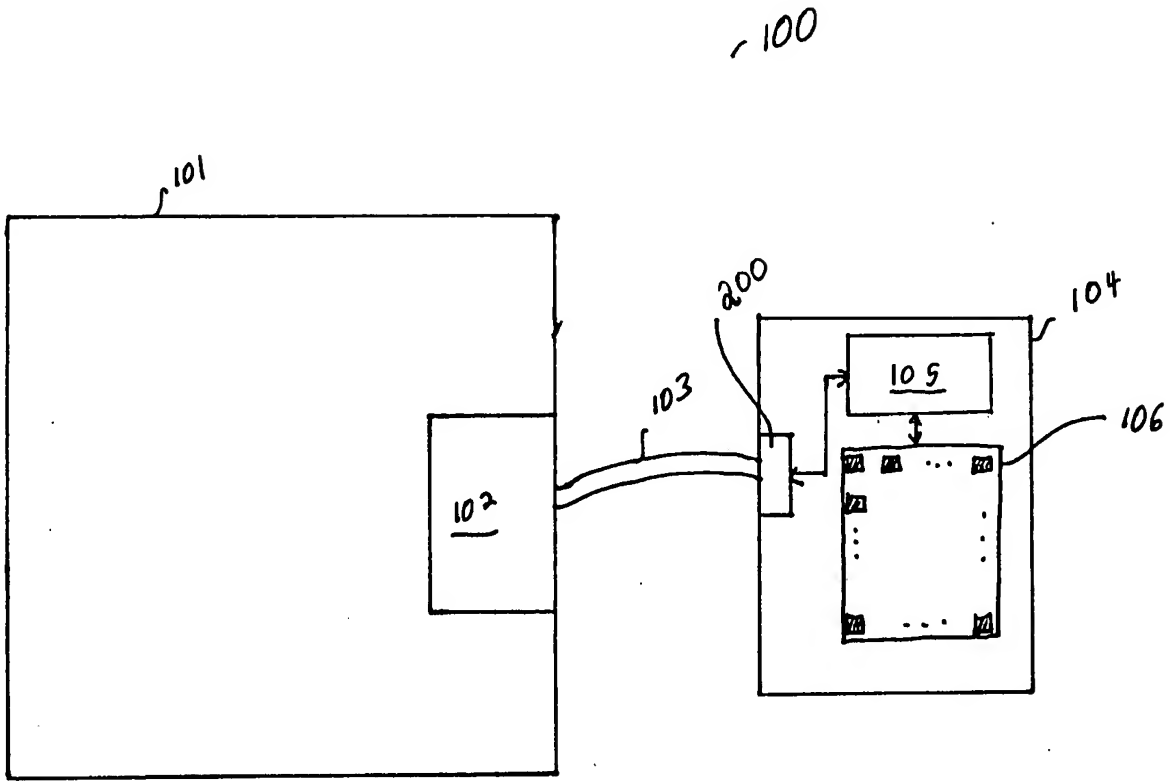


Figure 1

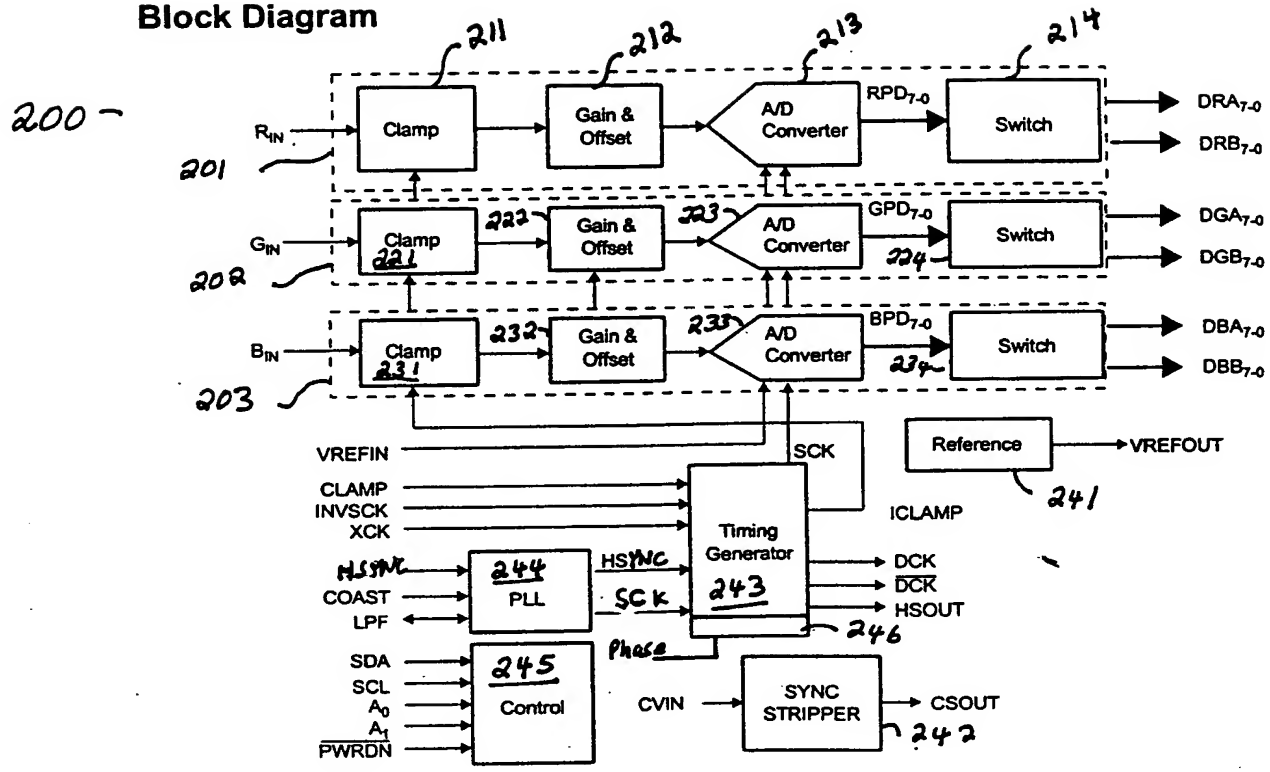


Figure 2a

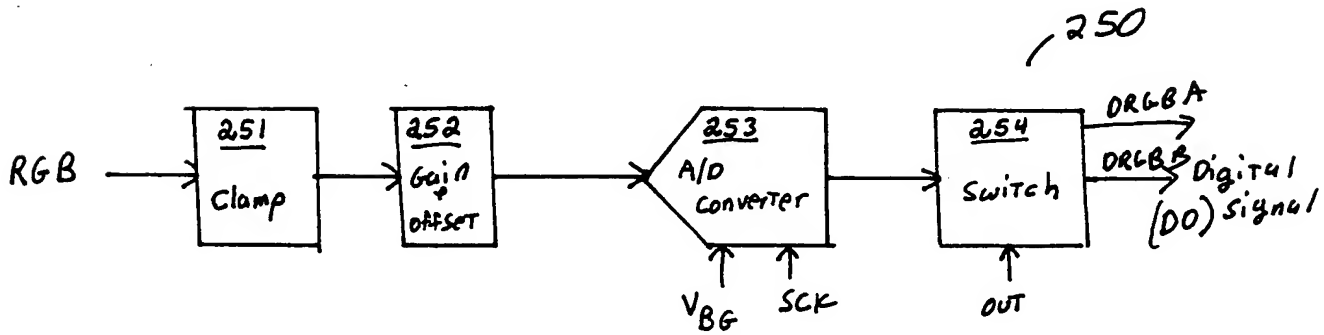


Figure 2b

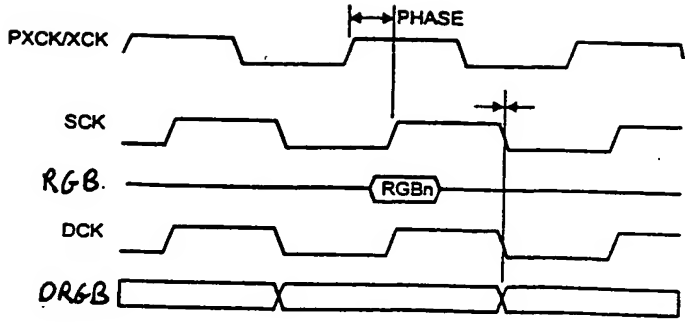


Figure 2c

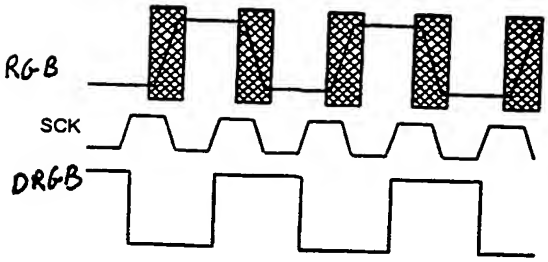


Figure 2d

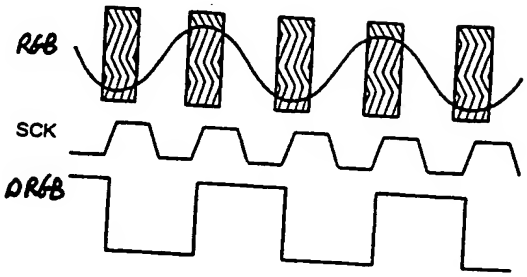


Figure 2e

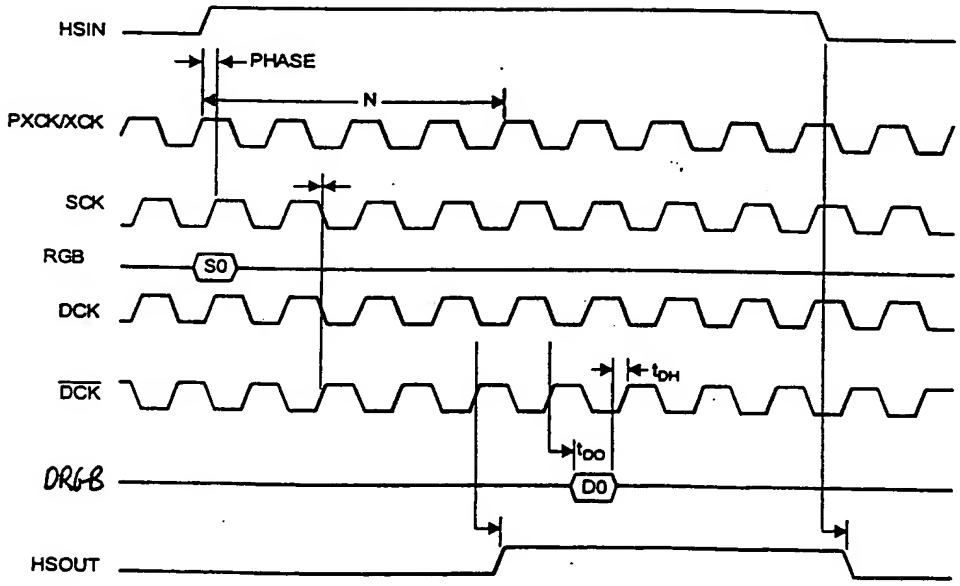


Figure 2f

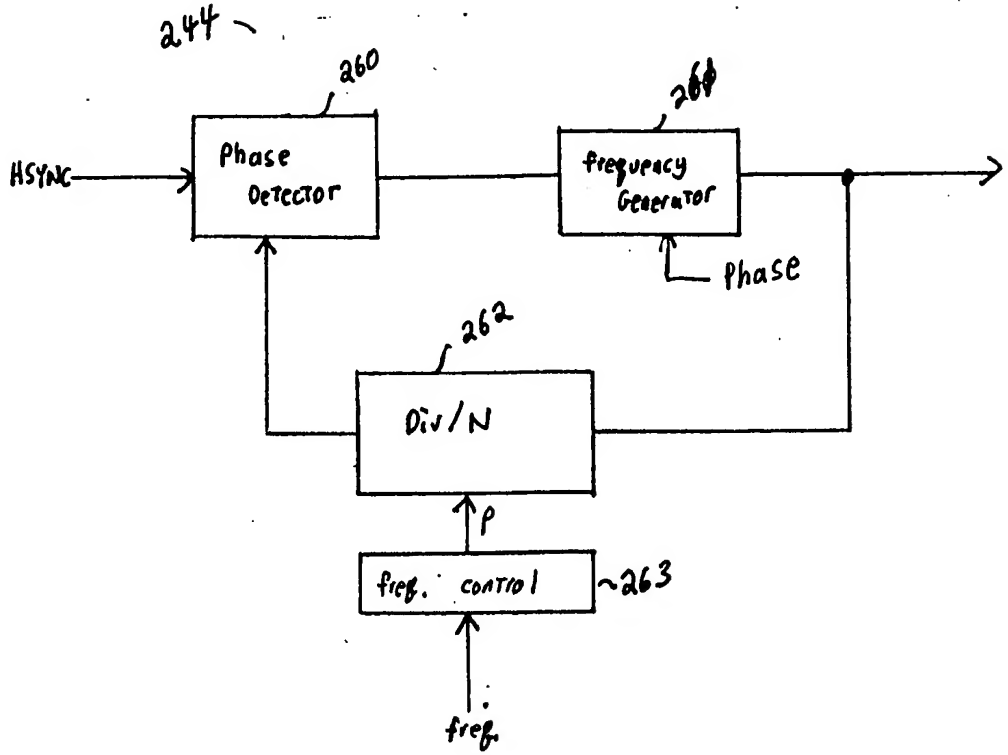

244
260
Phase
Detector
HSYNC
264
Frequency
Generator
Phase
262
Div/N
P
freq. control
263
freq.

Figure 2g

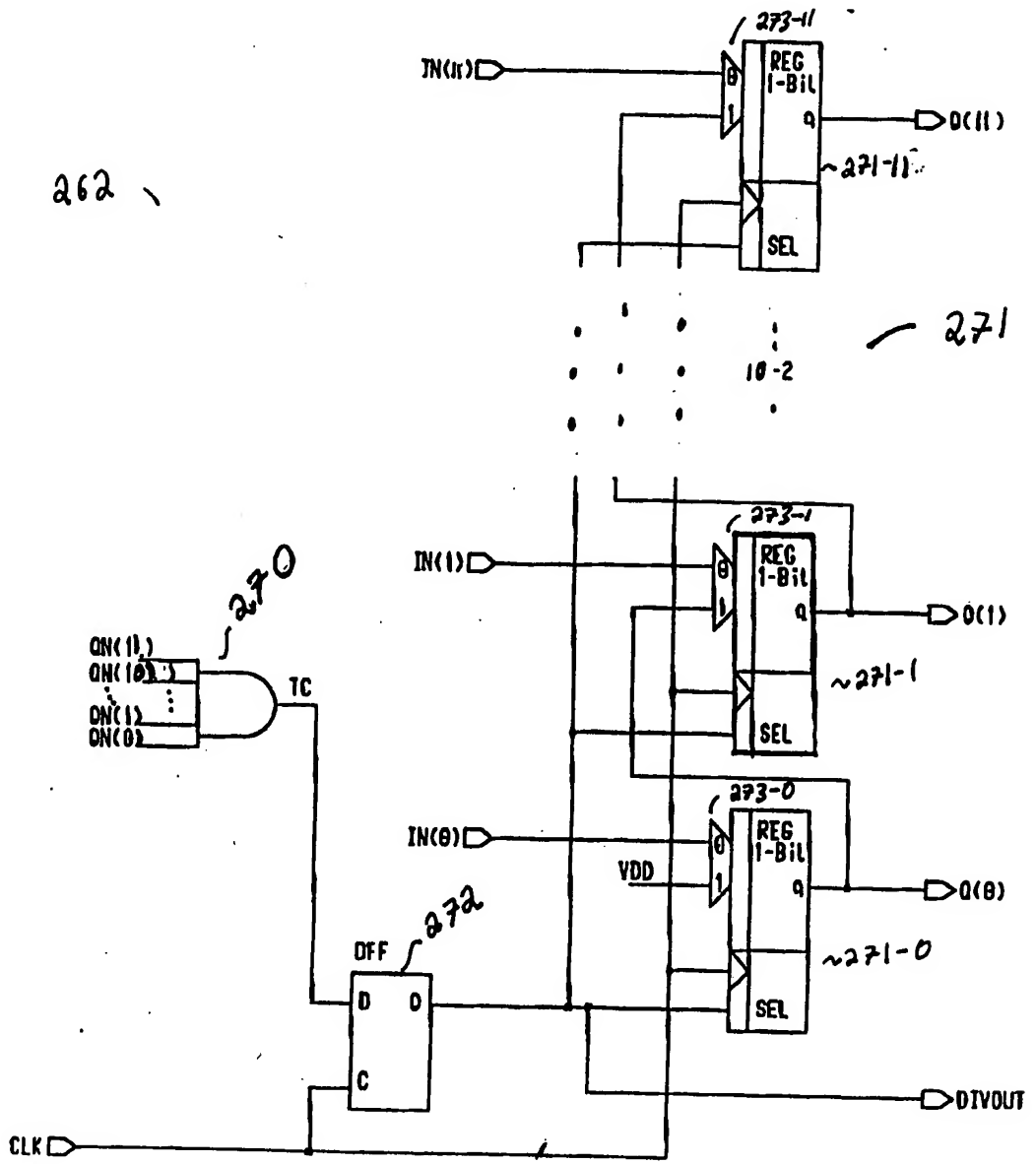

262
273-11
IN(11)
REG
1-Bit
D
Q
Q(11)
271-11
SEL
271
10-2
273-1
IN(1)
Q(1)
271-1
270
QN(11)
QN(10)
QN(1)
QN(0)
TC
273-0
IN(0)
VDD
Q(0)
271-0
272
DFF
D
Q
C
CLK
DIVOUT

Figure 2h

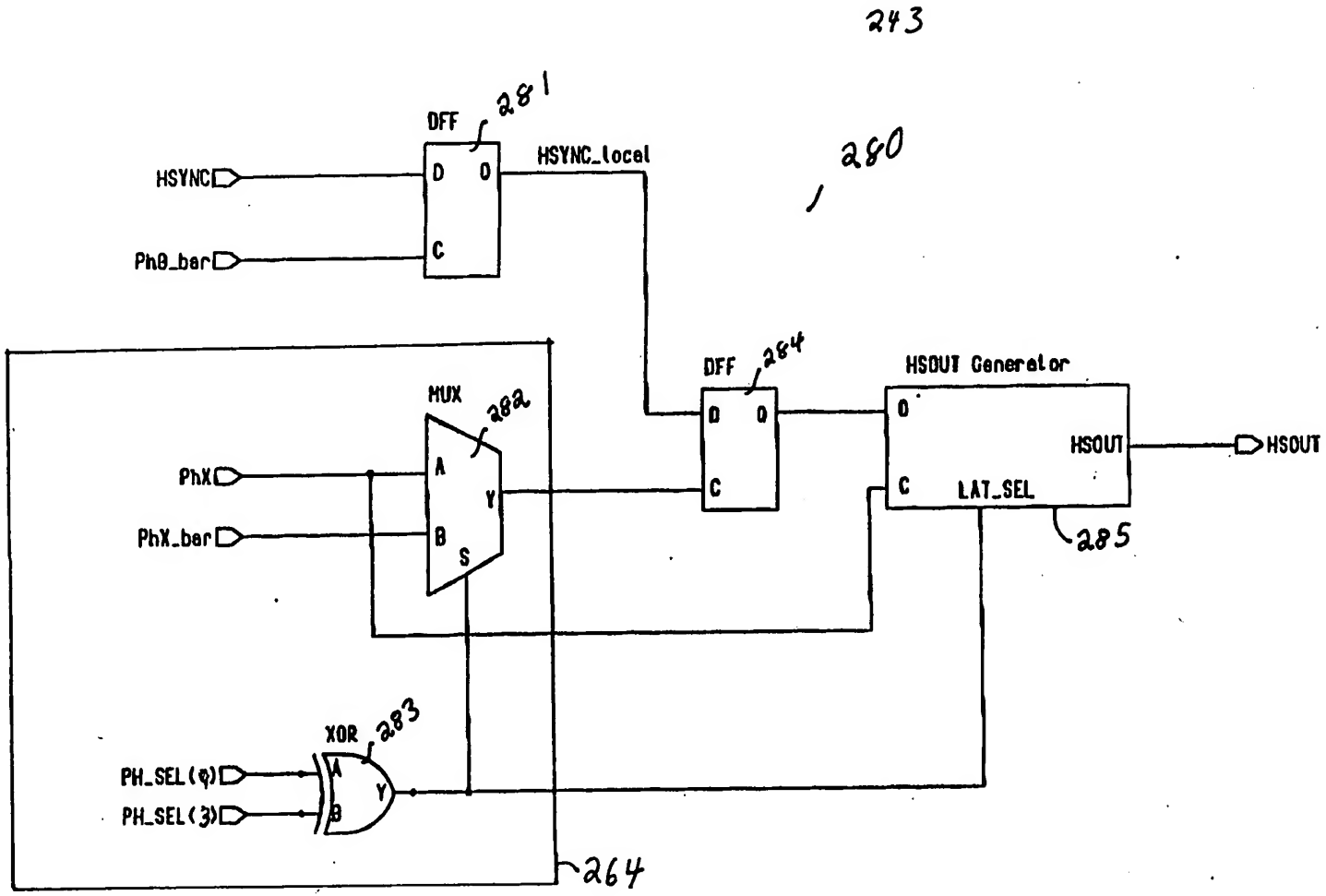

243
281
DFF
HSYNC
Ph0_bar
D
Q
C
HSYNC_local
280
MUX
282
PhX
PhX_bar
A
B
S
Y
DFF
284
D
Q
C
HSOUT Generator
D
C
HSOUT
LAT_SEL
285
HSOUT
XOR
283
PH_SEL(φ)
PH_SEL(3)
A
B
Y
264

Figure 2i

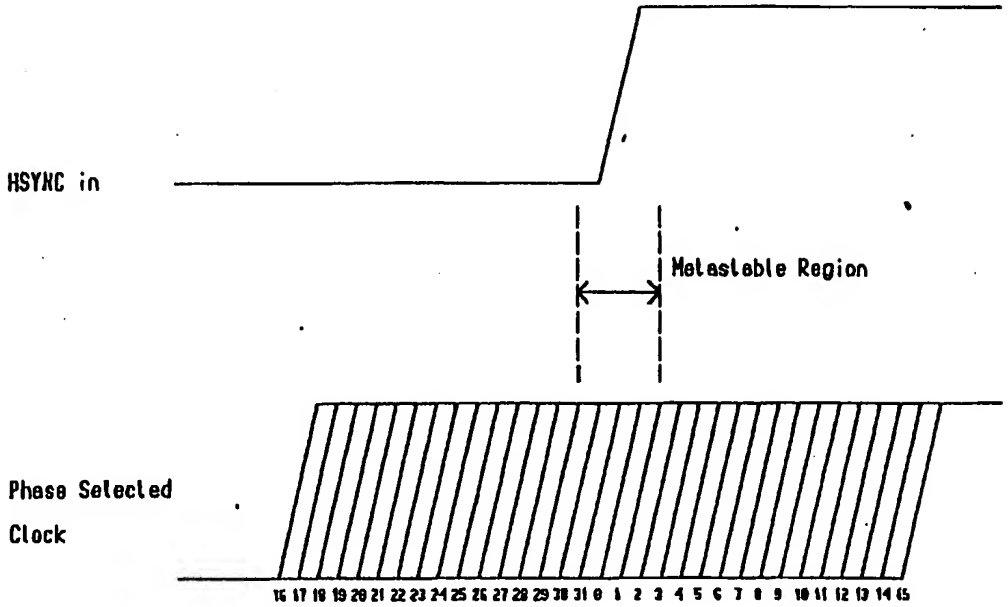

HSYNC in
Metastable Region
Phase Selected
Clock
16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Figure 2j

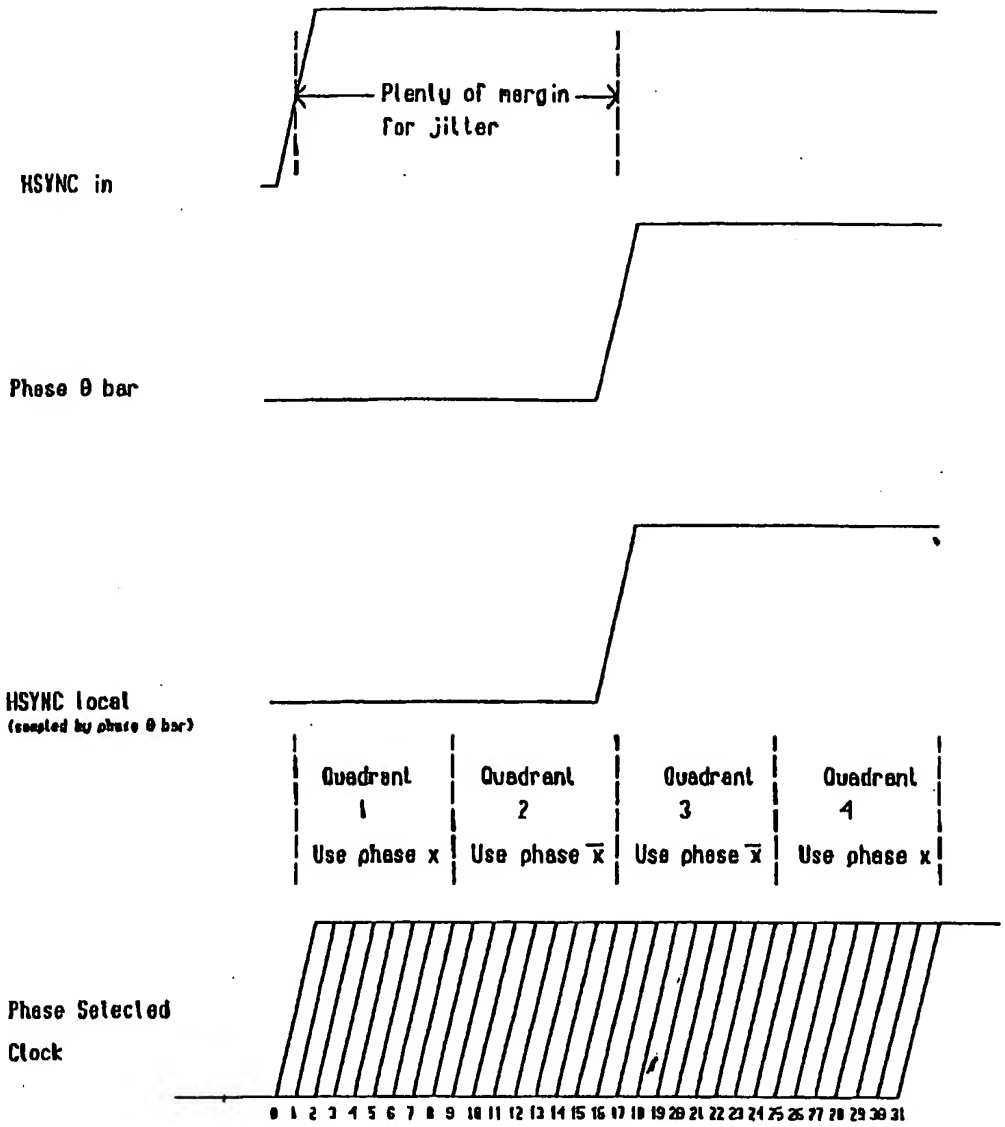
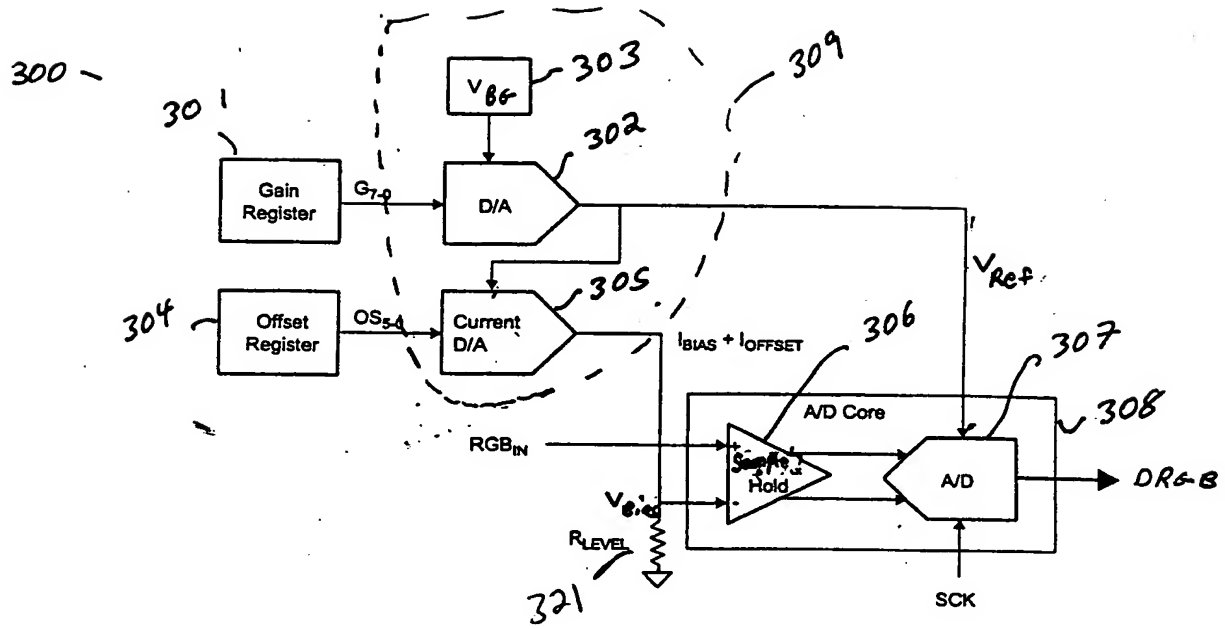

Plenty of margin for jitter
HSYNC in
Phase θ bar
HSYNC local
(sampled by phase θ bar)
Quadrant 1
Use phase x
Quadrant 2
Use phase x̄
Quadrant 3
Use phase x̄
Quadrant 4
Use phase x
Phase Selected Clock
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

Figure 2d

Figure 3a


300
301
303
309
302
Gain Register
G_{7-0}
D/A
V_{Ref}
304
Offset Register
OS_{5-0}
Current D/A
305
$I_{BIAS} + I_{OFFSET}$
306
307
308
A/D Core
RGB_{IN}
Sample & Hold
A/D
DRGB
V_{Black}
R_{LEVEL}
321
SCK

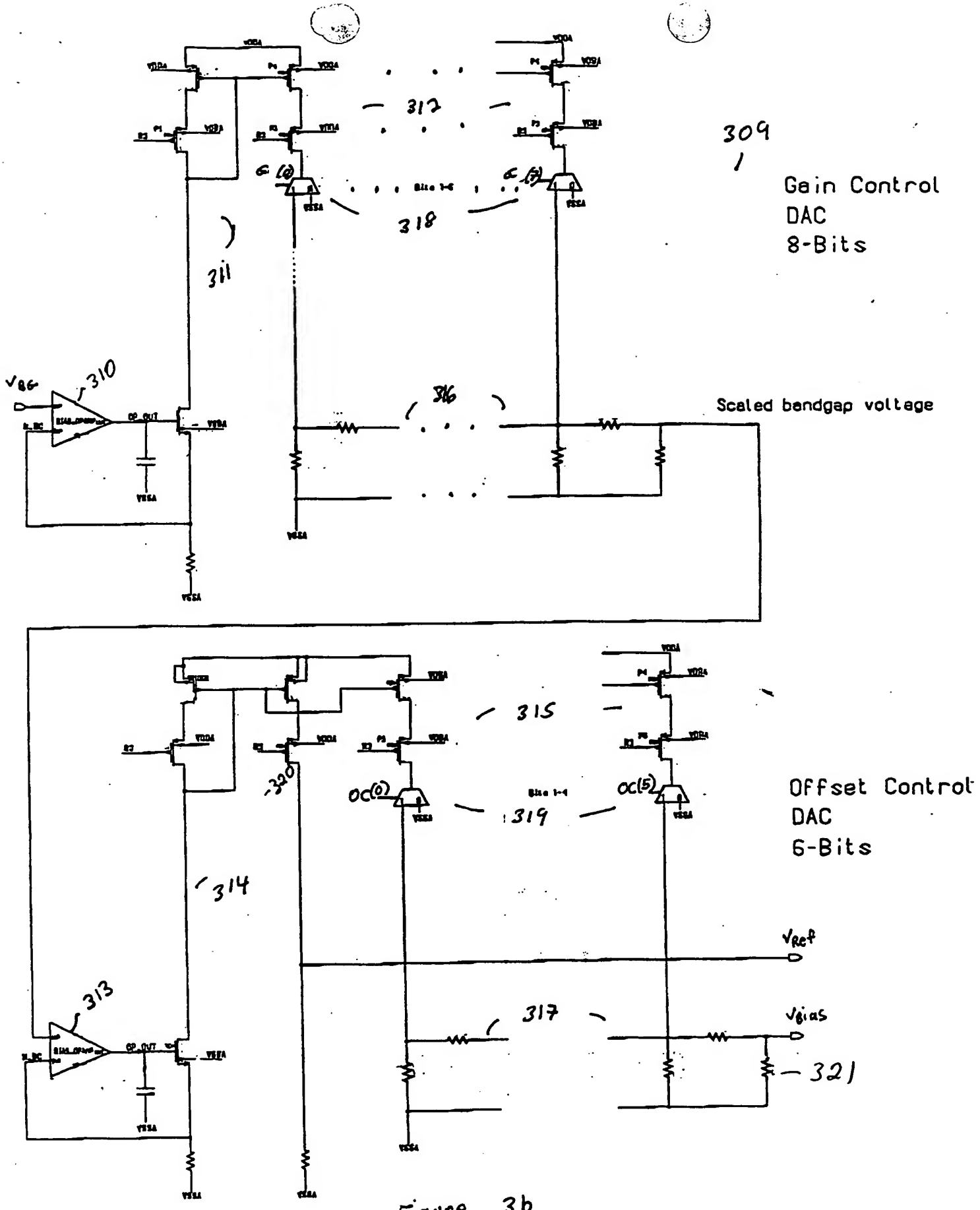

309
Gain Control
DAC
8-Bits
312
318
311
310
316
Scaled bandgap voltage
315
320
319
314
313
317
321
Offset Control
DAC
6-Bits

Figure 3b

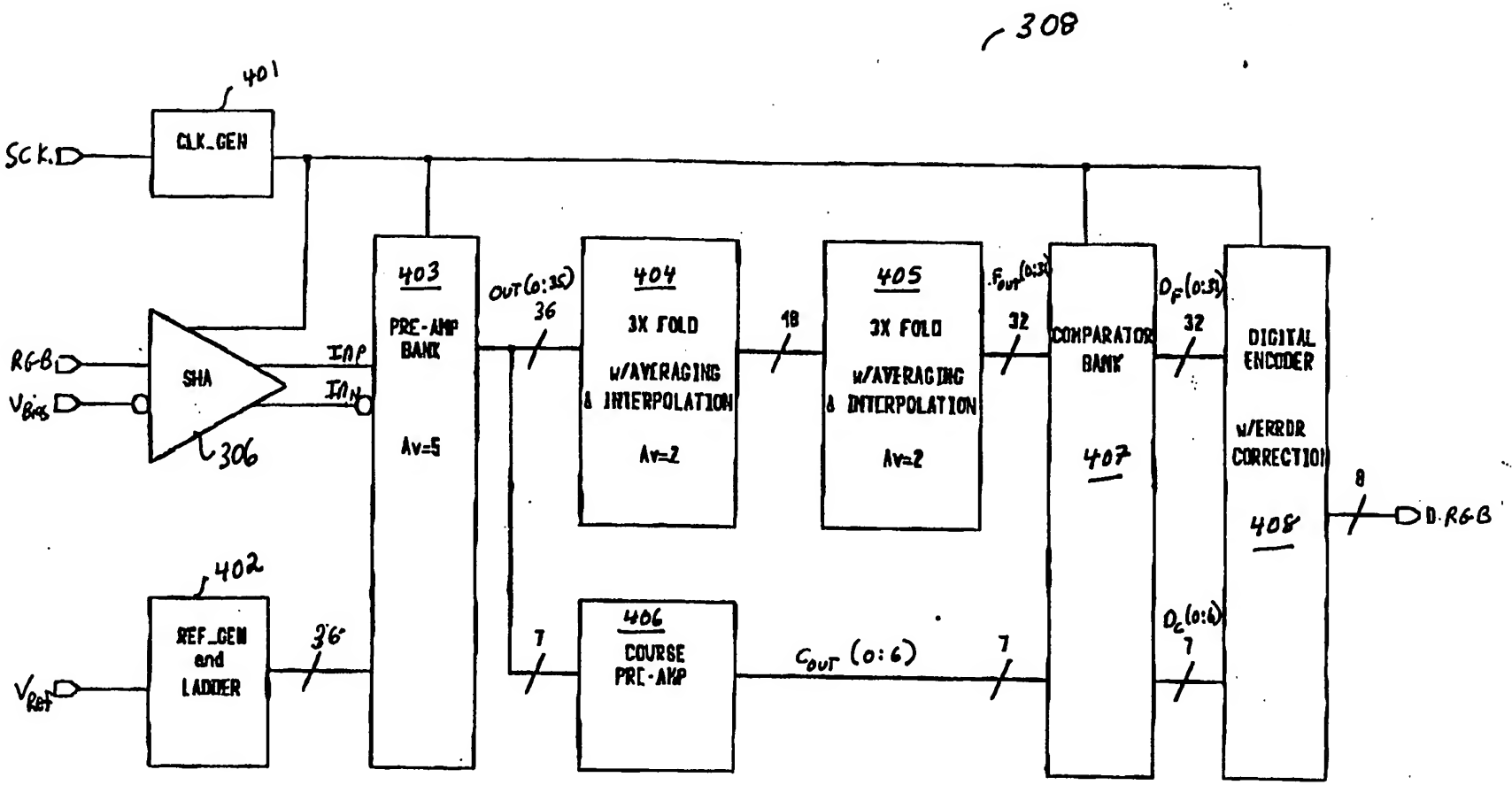

308
401
CLK_GEN
Sck
RGB
VBias
SHA
306
INP
INN
403
PRE-AMP BANK
Av=5
OUT(0:35)
36
404
3X FOLD
W/AVERAGING & INTERPOLATION
Av=2
18
405
3X FOLD
W/AVERAGING & INTERPOLATION
Av=2
FOUT(0:31)
32
COMPARATOR BANK
407
DF(0:31)
32
DIGITAL ENCODER
W/ERROR CORRECTION
408
8
D.RGB
402
REF_GEN and LADDER
VRef
36
7
406
COURSE PRE-AMP
COUT(0:6)
7
DC(0:6)
7

Figure 4a

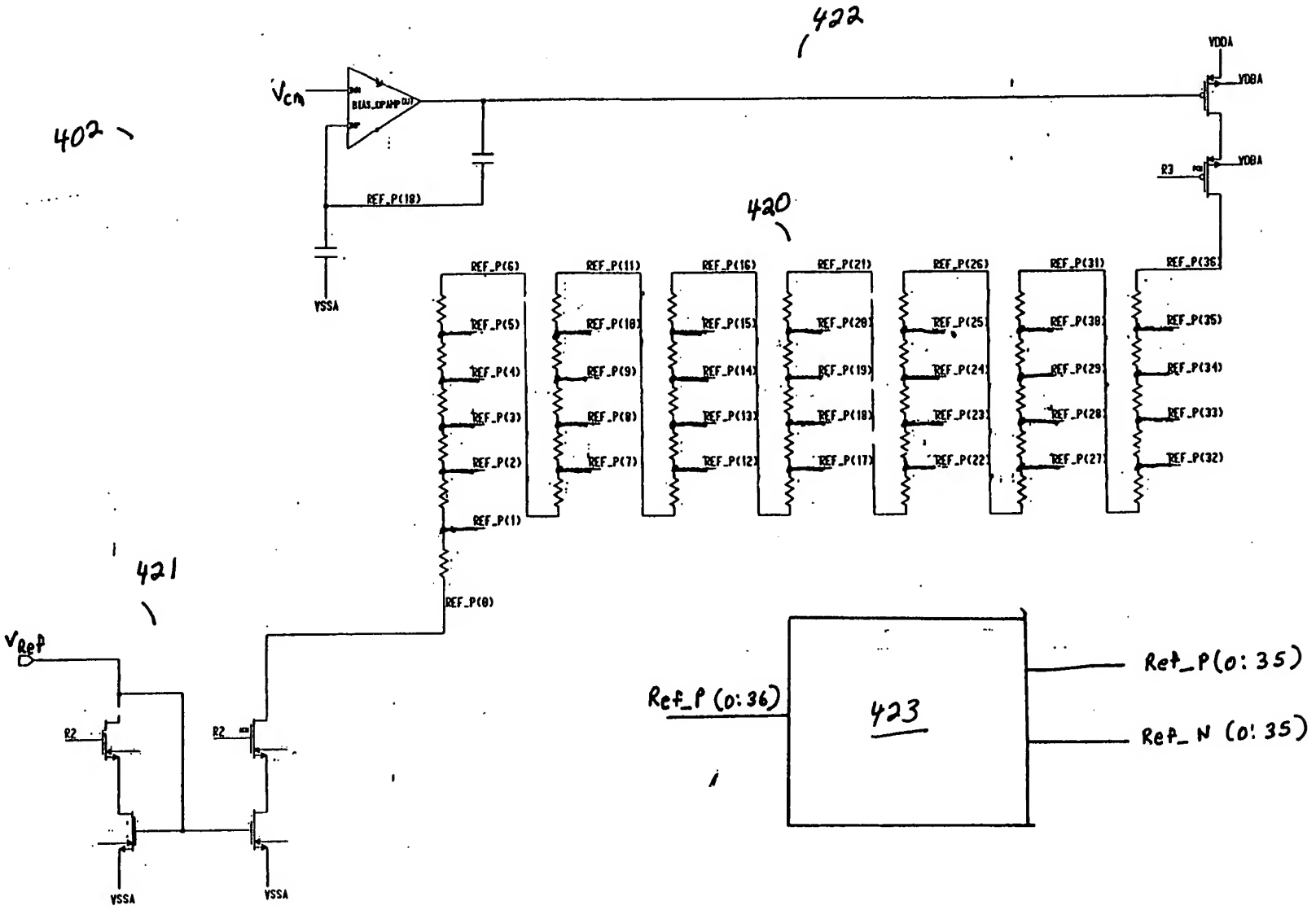

422
402
420
421
VCM
BIAS_OPAMP
OUT
VDDA
R3
REF_P(18)
VSSA
REF_P(6)
REF_P(11)
REF_P(16)
REF_P(21)
REF_P(26)
REF_P(31)
REF_P(36)
REF_P(5)
REF_P(10)
REF_P(15)
REF_P(20)
REF_P(25)
REF_P(30)
REF_P(35)
REF_P(4)
REF_P(9)
REF_P(14)
REF_P(19)
REF_P(24)
REF_P(29)
REF_P(34)
REF_P(3)
REF_P(8)
REF_P(13)
REF_P(18)
REF_P(23)
REF_P(28)
REF_P(33)
REF_P(2)
REF_P(7)
REF_P(12)
REF_P(17)
REF_P(22)
REF_P(27)
REF_P(32)
REF_P(1)
REF_P(0)
VRefP
R2
R2
VSSA
VSSA
Ref_P (0:36)
423
Ref_P(0:35)
Ref_N (0:35)

Figure 4b

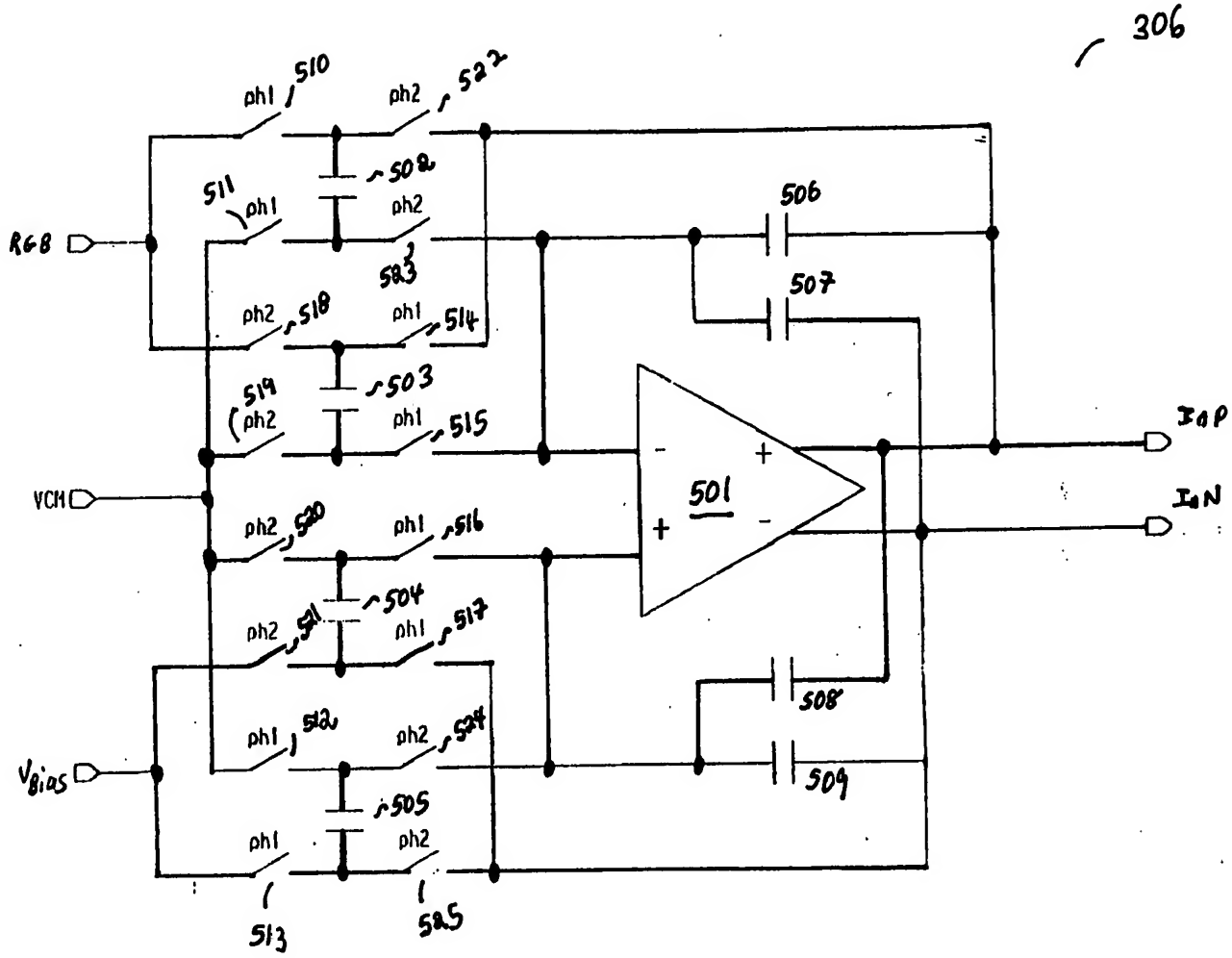

306
ph1
510
ph2
522
502
511
ph1
ph2
RGB
523
506
507
ph2
518
ph1
514
503
519
ph2
ph1
515
VCM
501
ph2
520
ph1
516
504
ph2
521
ph1
517
508
ph1
512
ph2
524
V_{Bias}
505
509
ph1
ph2
513
525
I_{OP}
I_{ON}

Figure 5

403

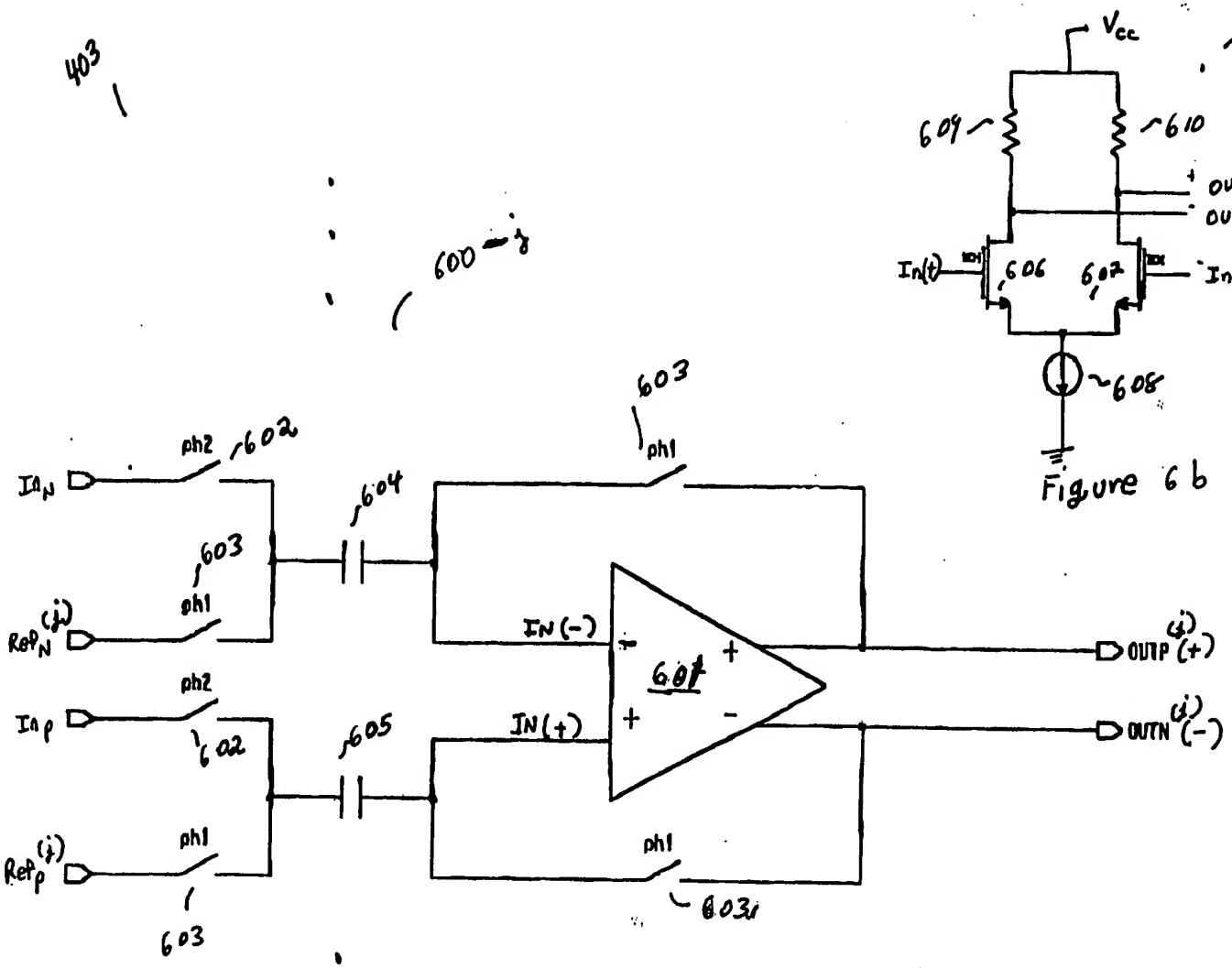
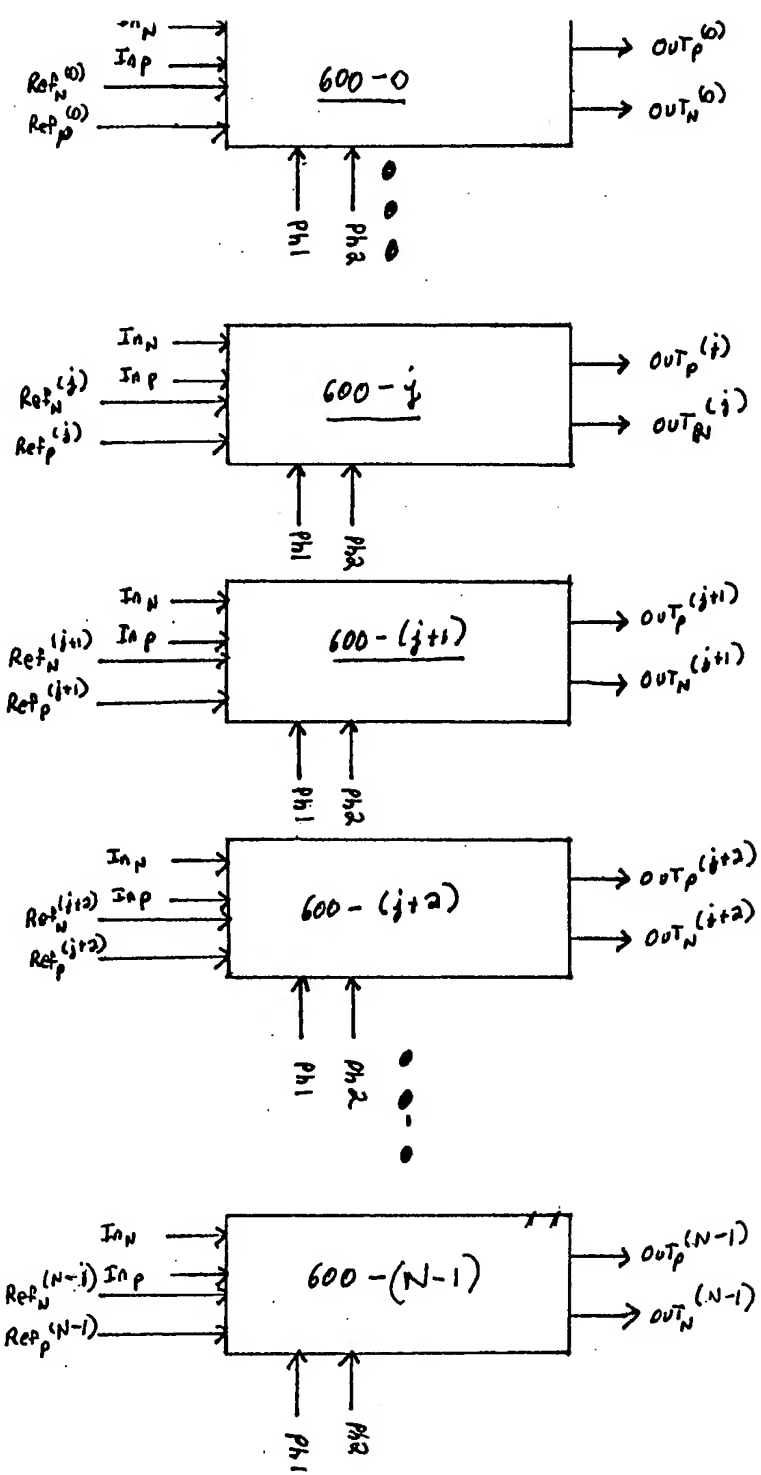


Figure 6a

Figure 6b



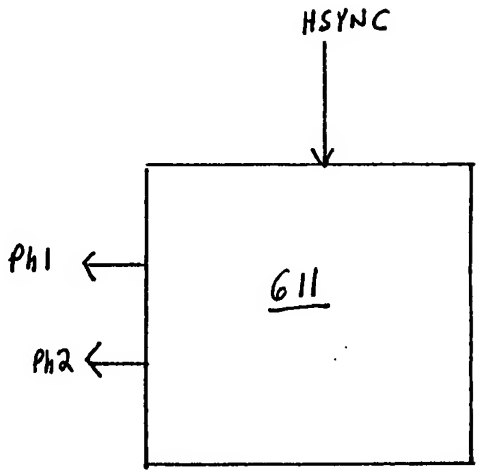


Figure 6C

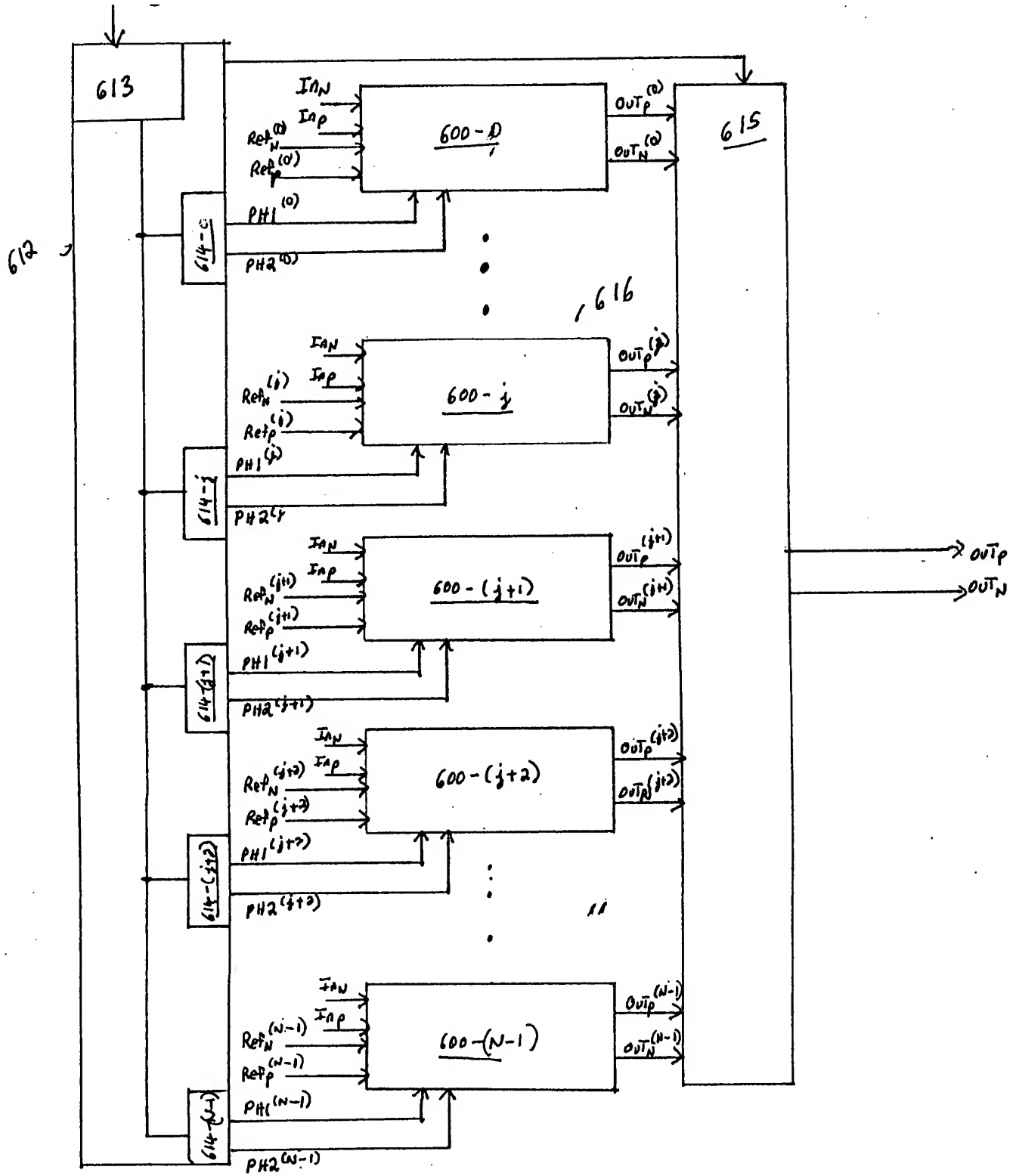

613
612
615
616
600-0
600-j
600-(j+1)
600-(j+2)
600-(N-1)
614-0
614-j
614-(j+1)
614-(j+2)
614-(N-1)
In_N
In_P
$Ref_N^{(0)}$
$Ref_P^{(0)}$
$PH1^{(0)}$
$PH2^{(0)}$
$OUT_P^{(0)}$
$OUT_N^{(0)}$
$Ref_N^{(j)}$
$Ref_P^{(j)}$
$PH1^{(j)}$
$PH2^{(j)}$
$OUT_P^{(j)}$
$OUT_N^{(j)}$
$Ref_N^{(j+1)}$
$Ref_P^{(j+1)}$
$PH1^{(j+1)}$
$PH2^{(j+1)}$
$OUT_P^{(j+1)}$
$OUT_N^{(j+1)}$
$Ref_N^{(j+2)}$
$Ref_P^{(j+2)}$
$PH1^{(j+2)}$
$PH2^{(j+2)}$
$OUT_P^{(j+2)}$
$OUT_N^{(j+2)}$
$Ref_N^{(N-1)}$
$Ref_P^{(N-1)}$
$PH1^{(N-1)}$
$PH2^{(N-1)}$
$OUT_P^{(N-1)}$
$OUT_N^{(N-1)}$
OUT_P
OUT_N

Figure 60

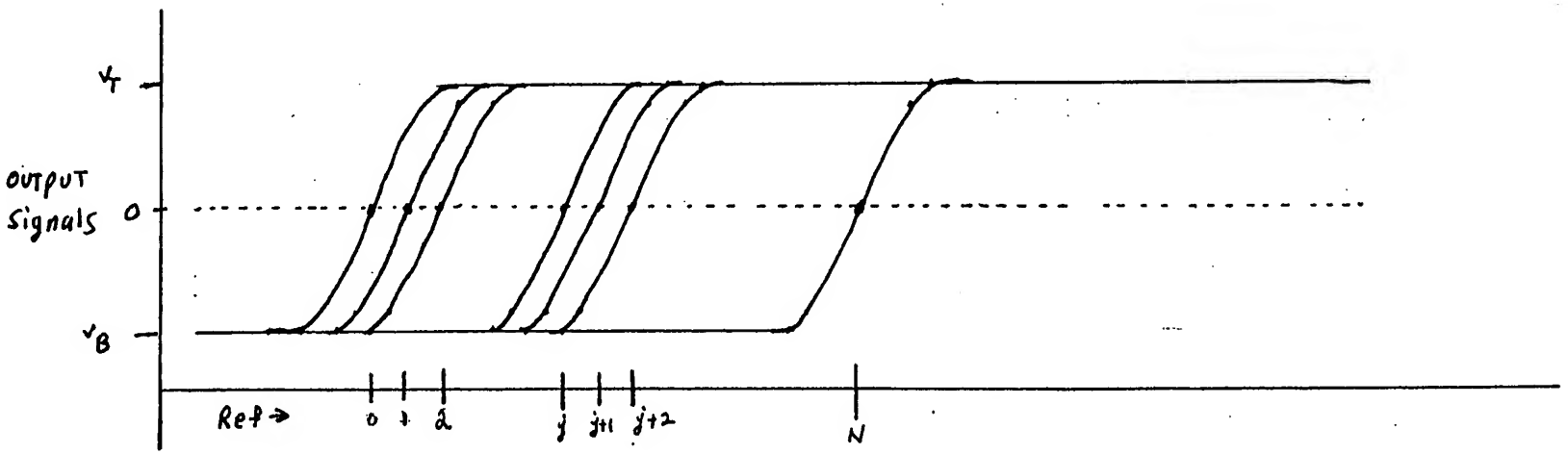


Figure 6E

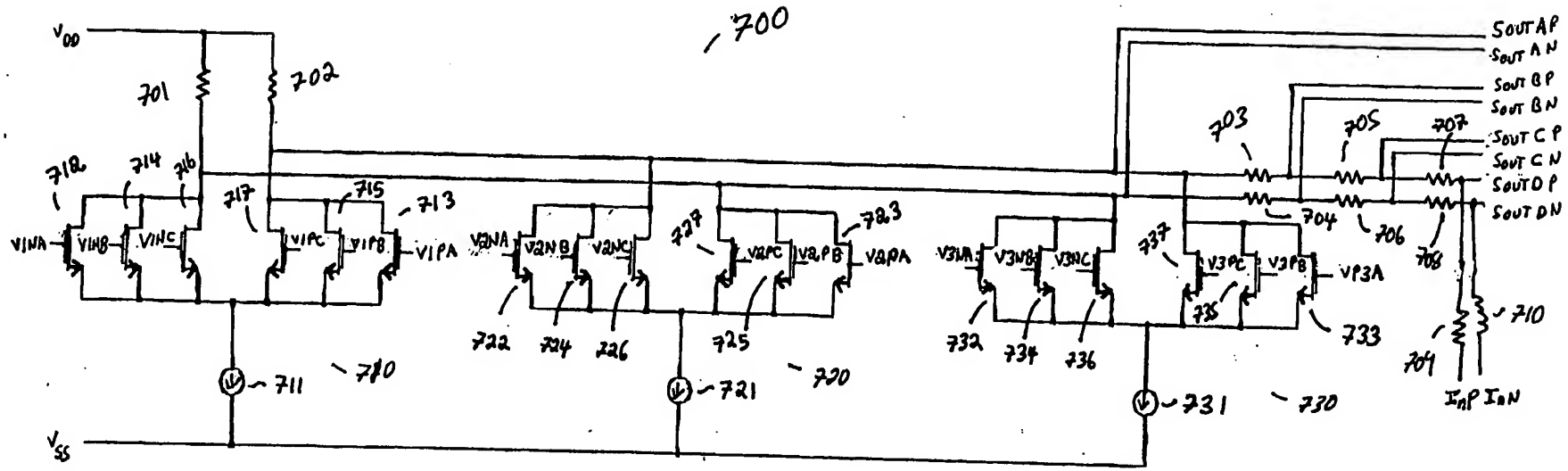


Figure 7a

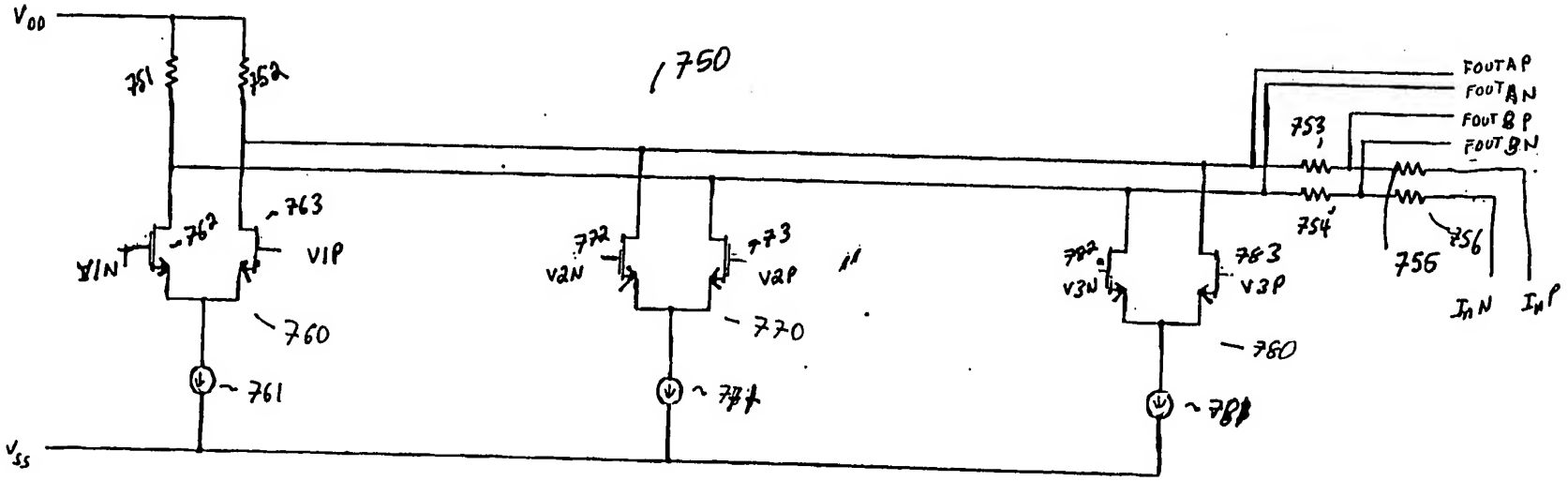


Figure 7b

Figure 7C

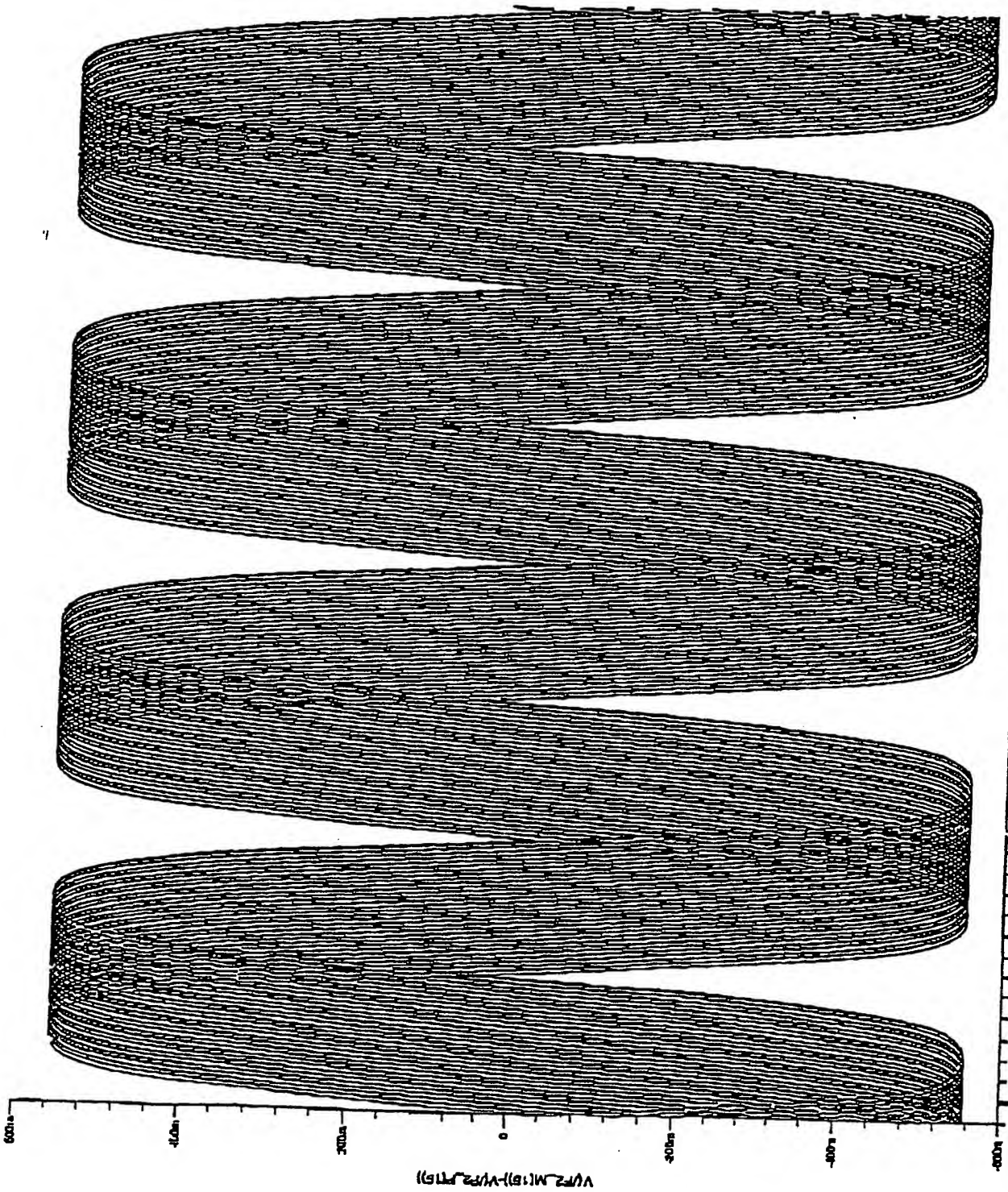


Figure 7D

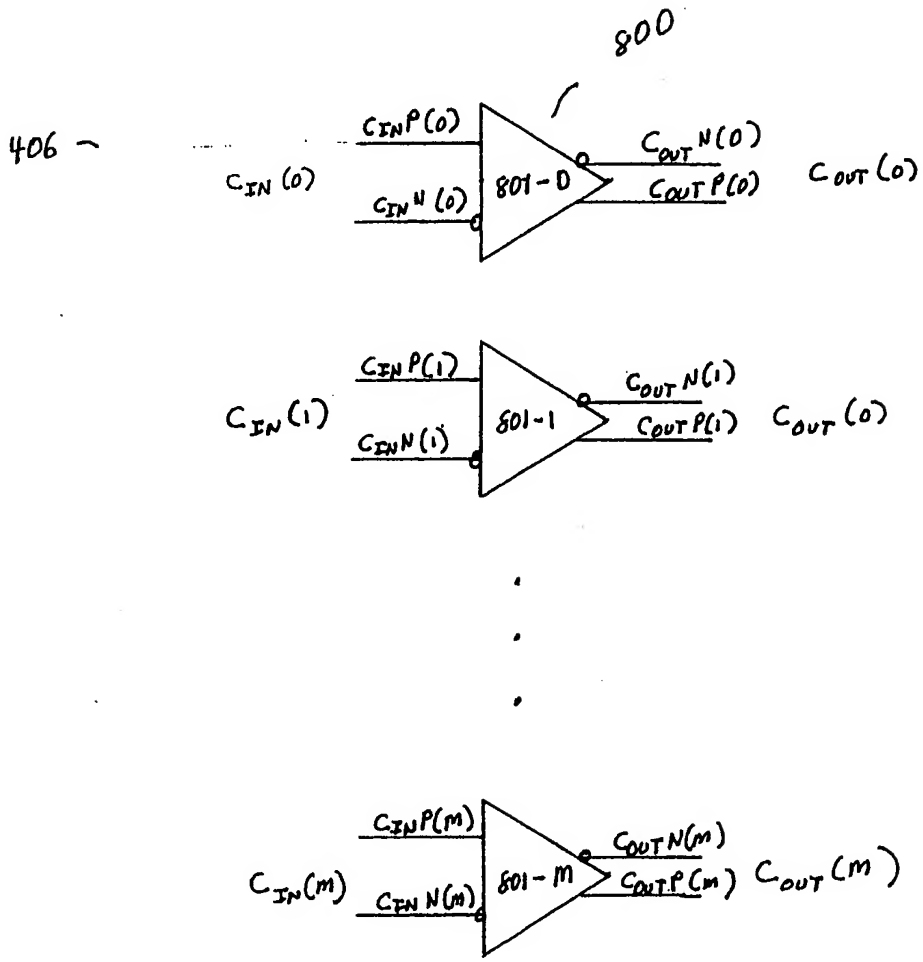

800
406
$C_{IN}(0)$
$C_{IN}P(0)$
$C_{IN}N(0)$
801-0
$C_{OUT}N(0)$
$C_{OUT}P(0)$
$C_{OUT}(0)$
$C_{IN}(1)$
$C_{IN}P(1)$
$C_{IN}N(1)$
801-1
$C_{OUT}N(1)$
$C_{OUT}P(1)$
$C_{OUT}(0)$
$C_{IN}(m)$
$C_{IN}P(m)$
$C_{IN}N(m)$
801-m
$C_{OUT}N(m)$
$C_{OUT}P(m)$
$C_{OUT}(m)$

Figure 8

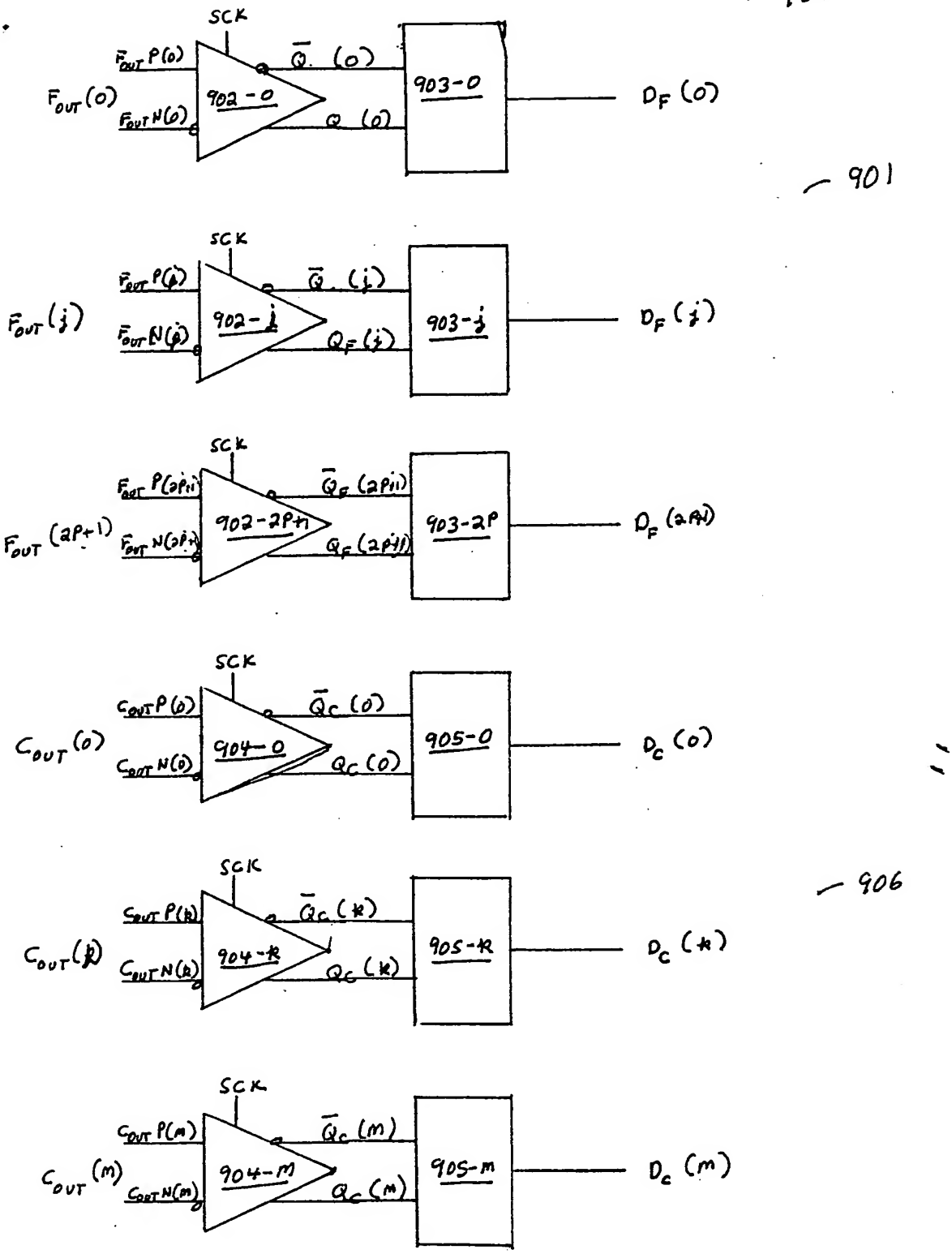

SCK
$F_{OUT}P(0)$
$F_{OUT}N(0)$
$F_{OUT}(0)$
$\bar{Q}_F(0)$
$Q_F(0)$
902-0
903-0
$D_F(0)$
901
SCK
$F_{OUT}P(j)$
$F_{OUT}N(j)$
$F_{OUT}(j)$
$\bar{Q}_F(j)$
$Q_F(j)$
902-j
903-j
$D_F(j)$
SCK
$F_{OUT}P(2P+1)$
$F_{OUT}N(2P+1)$
$F_{OUT}(2P+1)$
$\bar{Q}_F(2P+1)$
$Q_F(2P+1)$
902-2P+1
903-2P
$D_F(2P+1)$
SCK
$C_{OUT}P(0)$
$C_{OUT}N(0)$
$C_{OUT}(0)$
$\bar{Q}_C(0)$
$Q_C(0)$
904-0
905-0
$D_C(0)$
906
SCK
$C_{OUT}P(k)$
$C_{OUT}N(k)$
$C_{OUT}(k)$
$\bar{Q}_C(k)$
$Q_C(k)$
904-k
905-k
$D_C(k)$
SCK
$C_{OUT}P(m)$
$C_{OUT}N(m)$
$C_{OUT}(m)$
$\bar{Q}_C(m)$
$Q_C(m)$
904-m
905-m
$D_C(m)$

Figure 9

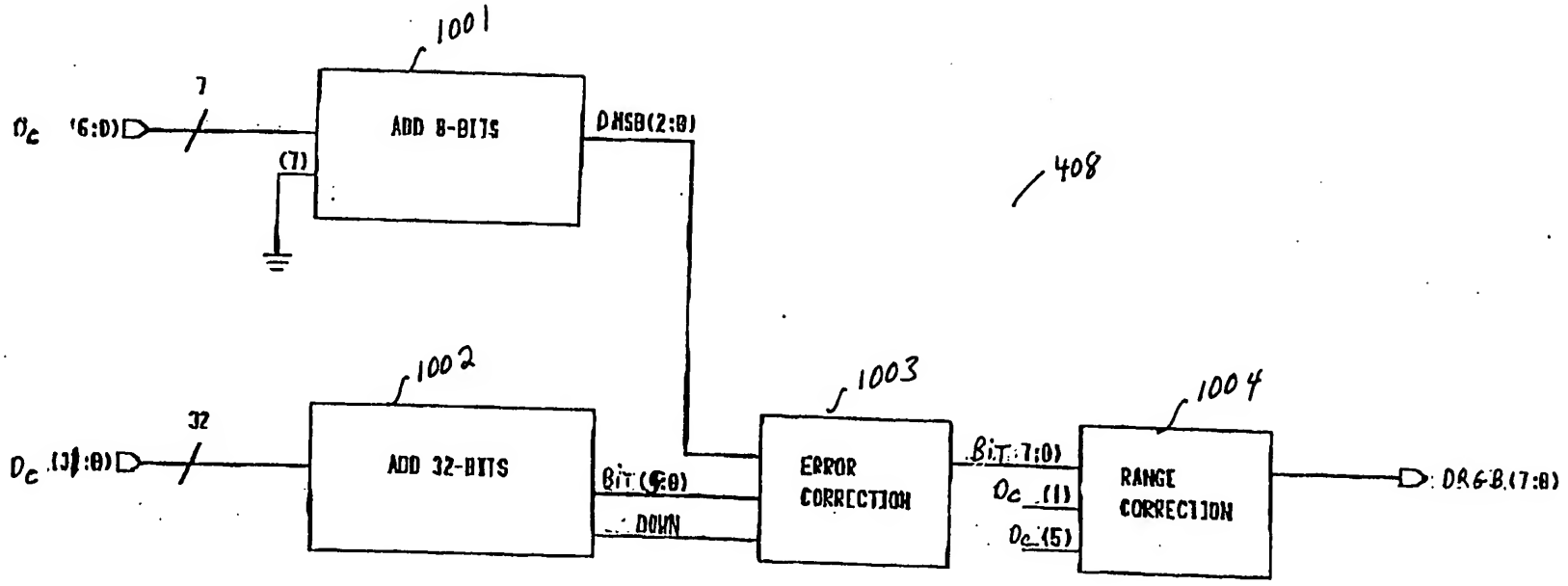

1001
7
Dc (6:0)
(7)
ADD 8-BITS
DMSB(2:8)
408
1002
32
Dc (31:8)
ADD 32-BITS
BIT (5:0)
DOWN
1003
ERROR CORRECTION
BIT 7:0)
Dc (1)
Dc (5)
1004
RANGE CORRECTION
DRGB(7:8)

Figure 10a

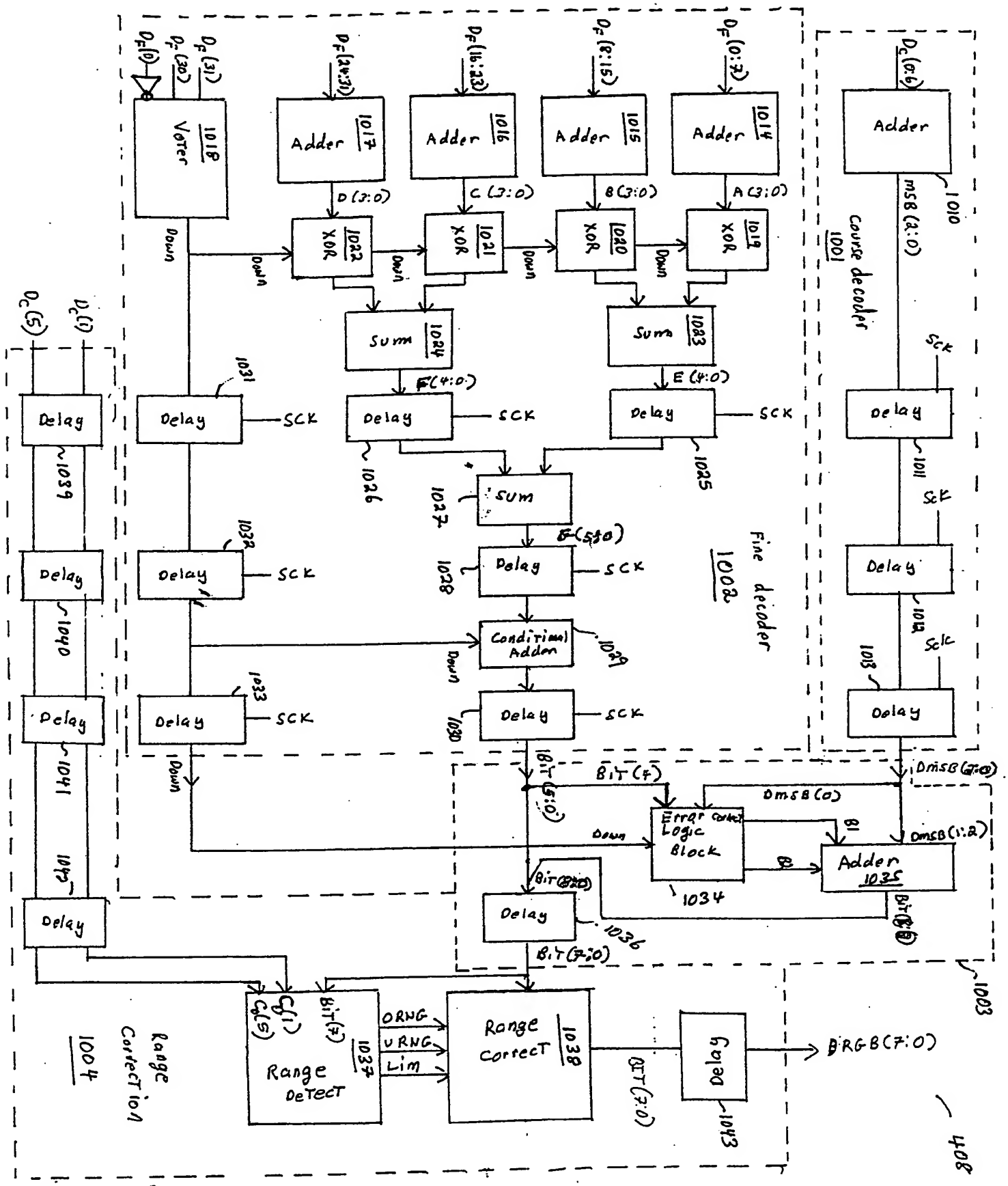

Adder 1017
Adder 1016
Adder 1015
Adder 1014
Voter 1018
XOR 1022
XOR 1021
XOR 1020
XOR 1019
Sum 1024
Sum 1023
Adder
Course decoder 1001
Fine decoder 1002
Delay
SCK
Conditional Adder 1029
Error correct Logic Block 1034
Adder 1035
Range Detect 1037
Range Correct 1038
Range Correct 1004
1003
408
BRGB(7:0)

Figure 10b